

Publications

■ Books

1. *Phase-Locked Loops: System Perspectives and Circuit Design Aspects*, W. Rhee and Z. Yu, Wiley-IEEE Press, Jan. 2024.
2. *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, Edited by W. Rhee, The Institution of Engineering and Technology (IET), June 2020.
3. *Wireless Transceiver Circuits: System Perspectives and Design Aspects*, Edited by W. Rhee, CRC Press, Feb. 2015.

■ Book Chapters

1. W. Rhee, "Evolution of monolithic phase-locked loops," in Chapter 1, *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, Edited by W. Rhee, The Institution of Engineering and Technology (IET), pp. 3-29, June 2020.
2. N. Xu, W. Rhee, and Z. Wang, "FIR filtering techniques for clock and frequency generation," in Chapter 10, *Mixed Signal Circuits*, Edited by T. Noulis and M. Soma, CRC Press, pp. 261-278, Oct. 2015.
3. N. Xu, W. Rhee, and Z. Wang, "Hybrid phase modulators with enhanced linearity," in Chapter 17, *Wireless Transceiver Circuits: System Perspectives and Design Aspects*, Edited by W. Rhee, CRC Press, pp. 445-466, Feb. 2015.
4. X. Yu, W. Rhee, and Z. Wang, " $\Delta\Sigma$ phase-locked loops," in Chapter 12, *CMOS Nanoelectronics: Analog and RF VLSI Circuits*, Edited by K. Iniewski, McGraw Hill Publishers, pp. 411-436, Sept. 2011.
5. W. Rhee, "Practical design aspects in fractional- N frequency synthesis," *Analog Circuit Design*, Edited by A. van Roermund, M. Steyaert, and J. Huijsing, Kluwer Academic Publishers, pp. 3-26, 2003.
6. W. Rhee, B. Song, and A. Ali, "A 1.1-GHz CMOS fractional- N frequency synthesizer with a 3-b third-order delta-sigma modulator," *Phase-Locking in High Performance Systems: From Devices to Architectures*, Edited by B. Razavi, John Wiley & Sons, Inc., pp. 596-602, 2003.

■ Articles

1. A. Altvater, "In Step With Woogeun Rhee: *Benefiting Humanity With Global Reach*," *IEEE Solid-State Circuits Magazine*, vol. 14, Issue 1, pp. 97-99, Jan. 2022.

■ Journals

1. L. Feng, Q. Liao, L. Kuang, J. Zhao, W. Rhee, and Z. Wang, "A 0.6-V fully-integrated BLE transmitter in 65-nm CMOS using a common-mode-ripple-cancelled hybrid PLL and a duty-cycle-controlled class-E/F2 PA achieving 25% system efficiency at 0 dBm," accepted for *IEEE Journal of Solid-State Circuits*.
2. Y. Nie, W. Rhee, and Z. Wang, "A 27.9-mW 802.15.4/4z 1T2R transceiver with FIR-embedded quadrature hybrid correlation and AoA localization," accepted for *IEEE Journal of Solid-State Circuits*.
3. X. Ji, J. Zhao, W. Rhee, and Z. Wang, "A polar phase-tracking receiver with two-point injection technique," *IEEE Journal of Solid-State Circuits*, no. 5, vol. 60, pp. 1529-1540, May 2025.

4. L. Feng, X. Ji, L. Kuang, Q. Liao, S. Han, J. Zhao, W. Rhee, and Z. Wang, "An ultra-low-voltage bias-current-free fractional-N hybrid PLL with voltage-mode phase detection and interpolation," *IEEE Journal of Solid-State Circuits*, no. 1, vol. 60, pp. 85-98, Jan. 2025.
5. L. Lin, B. Wang, W. Rhee, and Z. Wang, "A 7.5-GHz frequency-hopping CDMA UWB transceiver for secure multi-sensor connectivity," *IEEE Trans. Circuits and Systems II*, vol. 69, pp. 163-167, Jan., 2025.
6. J. Zhao, W. Rhee, and Z. Wang, "A wide tracking range heterodyne phase-tracking receiver with 1-bit phase-domain demodulation," *IEEE Trans. Circuits and Systems I*, vol. 72, pp. 6459-6469, Dec. 2024.
7. Y. Nie, W. Rhee, and Z. Wang, "An IEEE 802.15.4/z coherent quadrature hybrid correlation UWB receiver in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 59, pp. 2378-2389, Aug. 2024.
8. B. Zhou, Y. Li, Z. Wang, C. Wang, W. Rhee, and Z. Wang, "A low-complexity FM-UWB transmitter with digital reuse and analog stacking," *IEEE Journal of Solid-State Circuits*, vol. 59, pp. 2121-2132, July 2024.
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10. B. Wang, C. Ding, Y. Nie, W. Rhee, and Z. Wang, "A 0.14-nJ/b 200-Mb/s 2.7–3.5-GHz quasi-balanced FSK transceiver with PLL-based modulation and sideband energy detection," *IEEE Trans. Circuits and Systems I*, vol. 71, pp. 1590-1601, Apr. 2024.
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13. L. Feng, W. Rhee, and Z. Wang, "A Quantization noise reduction method for delta-sigma fractional-N PLLs using cascaded injection-locked oscillators," *IEEE Trans. Circuits and Systems II*, vol. 69, pp. 2448-2452, May 2022.
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