Publications

- Books
  1. *Phase-Locked Loops: System Perspectives and Circuit Design Aspects,* W. Rhee and Z. Yu, Wiley-IEEE Press, Nov. 2023 (exp.)
  2. *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems,* Edited by W. Rhee, The Institution of Engineering and Technology (IET), June 2020.
  3. *Wireless Transceiver Circuits: System Perspectives and Design Aspects,* Edited by W. Rhee, CRC Press, Feb. 2015.

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  1. W. Rhee, "Evolution of monolithic phase-locked loops," in Chapter 1, *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems, Edited by W. Rhee, The Institution of Engineering and Technology (IET),* pp. 3-29, June 2020.
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- Invited Talks in International Conferences & Workshops
  1. W. Rhee, "PLL architectures, tradeoffs, and key application considerations," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2021. (online)
  2. W. Rhee, "Single-bit delta-sigma modulation techniques for robust communication systems," *IEEE International Conference on ASIC (ASICON), Chongqing,* China, Oct. 2019.
  3. W. Rhee, "Single-bit delta-sigma modulation techniques for robust wireless systems," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, May 2019.
  4. W. Rhee, "Energy-efficient proprietary transceivers for IoT and smartphone-based WPAN," *IEEE International Microwave Symposium (IMS) Workshop*, Philadelphia, Pennsylvania, June 2018.
  5. W. Rhee, "Phase-locked frequency synthesis and modulation," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018.
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10. W. Rhee, “Phase-locked clock generation for SoC: Circuit and system design aspects,” *IEEE International System-on-Chip Conference (SOCC)*, Beijing, China, September 2015.
11. W. Rhee, “Phase-locked clocking and frequency synthesis - System perspectives tailored for IC designers,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015.
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14. W. Rhee, “Ultra-wideband technology for short-range communications,” *Solid-State Devices and Materials (SSDM)*, Tsukuba, Japan, Sept. 2014.
15. W. Rhee, “Frequency synthesizers: From basics to advanced bundle,” *IEEE Asian Solid-State Circuits Conference (A-SSCC) Tutorial*, Singapore, Nov. 2013.
16. W. Rhee, X. Chen, and Z. Wang, “Delta-sigma ranging method for UWB radar systems,” *CMOS Emerging Technologies*, Whistler, Canada, July, 2013.
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18. W. Rhee, “Frequency synthesizers and PLL,” *IEEE International Conference on Solid-State and Integrated-Circuit Technology (ICSICT) Tutorial*, Beijing, China, Oct. 2008.
19. W. Rhee, “Clocking frequencies and spectralizing clocks in SoC design,” *International SoC Design Conference (ISOCC) Tutorial*, Seoul, Korea, Oct. 2007.
20. W. Rhee, “Practical design aspects in fractional-*N* frequency synthesis,” *12th Workshop on Advances in Analog Circuit Design*, Graz, Austria, Apr. 2003.
21. D. Wilson, W. Rhee, and B. S. Song, “Integrated RF receiver front ends and frequency synthesizers for wireless,” *Emerging Technologies: Designing Low Power Digital Systems, Tutorial Workshops in IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 369-396, June, 1996.

- IEEE DL Talks & Webinar
  1. W. Rhee, "Phase-locked loops: System perspectives tailored for IC designers," *IEEE SSCS Webinar Series*, Nov. 2017.
  2. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in SSCS Kansai Chapter*, Dec. 2017.
  3. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in New South Wales Chapter*, Aug. 2017.
  4. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in SSCS Austin Chapter*, May 2017.
  5. W. Rhee, “Phase-locked frequency synthesis and modulation for modern wireless transceivers,” *IEEE Distinguished Lecture Series in SSCS Atlanta Chapter*, Apr. 2017.
  6. W. Rhee, “Phase-locked clocking and frequency synthesis for wireline and wireless - System perspectives tailored for IC designers,” *IEEE Distinguished Lecture Series in SSCS UAE Chapter*, Oct. 2016.
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- Patents
  24 U.S. patents issued.

- Ph.D. Thesis
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